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Inventor Name Search Result

Your Search was:

Last Name = KOMODA
First Name = MICHIO

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07878614	5379232	150	05/05/1992	LOGIC SIMULATOR	KOMODA, MICHIO
07907054	Not Issued	161	07/01/1992	MASTER SLICE LSI WITH FAULT DETECTION CIRCUITRY	KOMODA, MICHIO
07929828	5515291	150	08/14/1992	APPARATUS FOR CALCULATING DELAY TIME IN LOGIC FUNCTIONAL BLOCKS	KOMODA, MICHIO
08007148	5347178	250	01/21/1993	CMOS SEMICONDUCTOR LOGIC CIRCUIT WITH MULTIPLE INPUT GATES	KOMODA, MICHIO
08049412	Not Issued	161	04/20/1993	SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF DESIGNING TEST PATTERN FOR THE SAME	KOMODA, MICHIO
08100117	5473548	150	07/30/1993	APPARATUS FOR COMPUTING POWER CONSUMPTION OF MOS TRANSISTOR LOGIC FUNCTION BLOCK	KOMODA, MICHIO
08100992	5438524	250	08/03/1993	LOGIC SYNTHESIZER	KOMODA, MICHIO
08212788	5541861	150	03/15/1994	LOGIC SIMULATOR	KOMODA, MICHIO
08212926	5444647	150	03/15/1994	MULTIPLIER CIRCUIT AND DIVISION CIRCUIT WITH A ROUND-OFF FUNCTION	KOMODA, MICHIO
08432924	Not Issued	161	05/01/1995	MASTER SLICE LSI WITH FAULT DETECTION CIRCUITRY	KOMODA, MICHIO
08433013	5619440	150	05/03/1995	MULTIPLIER CIRCUIT WITH ROUNDING-OFF FUNCTION	KOMODA, MICHIO

08757109	5729126	250	12/02/1996	MASTER SLICE LSI WITH INTEGRATED FAULT DETECTION CIRCUITRY	KOMODA, MICHIO
08915079	6510404	150	08/20/1997	GATE DELAY CALCULATION APPARATUS AND METHOD THEREOF USING PARAMETER EXPRESSING RC MODEL SOURCE RESISTANCE VALUE	KOMODA, MICHIO
08956872	6000050	150	10/23/1997	METHOD FOR MINIMIZING GROUND BOUNCE DURING DC PARAMETRIC TESTS USING BOUNDARY SCAN REGISTER	KOMODA, MICHIO
09037037	6076178	150	03/09/1998	TEST CIRCUIT AND METHOD FOR DC TESTING LSI CAPABLE OF PREVENTING SIMULTANEOUS CHANGE OF SIGNALS	KOMODA, MICHIO
09100025	6073265	150	06/19/1998	PIPELINE CIRCUIT WITH A TEST CIRCUIT WITH SMALL CIRCUIT SCALE AND AN AUTOMATIC TEST PATTERN GENERATING METHOD FOR TESTING THE SAME	KOMODA, MICHIO
09377037	6678849	150	08/19/1999	SEMICONDUCTOR INTEGRATED CIRCUIT AND TEST PATTERN GENERATION METHOD THEREFOR	KOMODA, MICHIO
09453795	6292043	150	12/03/1999	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH CORE POSITIONED CLOCK BUFFER AND PAD	KOMODA, MICHIO
09497172	6546537	150	02/03/2000	WIRING DATA GENERATION METHOD AND WIRING DATA GENERATION APPARATUS ALLOWING INCONSISTENCY BETWEEN BLOCK INTERNAL LINES AND BLOCK EXTERNAL LINES	KOMODA, MICHIO
09878352	6552551	150	06/12/2001	METHOD OF PRODUCING LOAD FOR DELAY TIME CALCULATION AND RECORDING MEDIUM	KOMODA, MICHIO
09879197	Not Issued	71	06/13/2001	Delay time estimation method and recording medium storing	KOMODA, MICHIO

				estimation program	
09921604	6925624	150	08/06/2001	CIRCUIT MODIFICATION METHOD	KOMODA, MICHIO
09970878	Not Issued	93	10/05/2001	METHOD OF FORMULATING LOAD MODEL FOR GLITCH ANALYSIS AND RECORDING MEDIUM WITH THE METHOD RECORDED THEREON	KOMODA, MICHIO
10133672	Not Issued	161	04/29/2002	Gate delay calculation apparatus and method thereof using parameter expressing RC model source resistance value	KOMODA, MICHIO
10141923	Not Issued	161	05/10/2002	Linear Filter circuit	KOMODA, MICHIO
11174542	Not Issued	20	07/06/2005	Delay calculation method capable of calculating delay time with small margin of error	KOMODA, MICHIO
11205149	Not Issued	20	08/17/2005	Automatic-arrangement-wiring apparatus for and program for performing layout of integrated circuit	KOMODA, MICHIO

Inventor Search Completed: No Records to Display.

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